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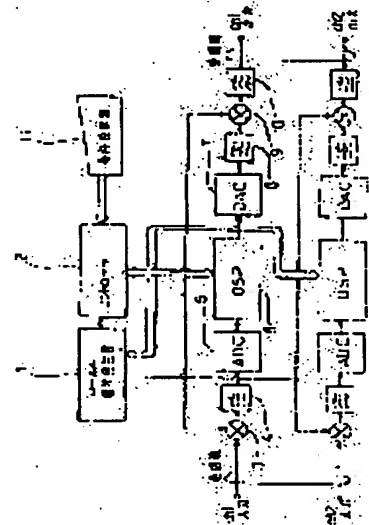
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(54) MULTI-PATH FADING SIMULATOR

(57)Abstract:

PURPOSE: To realize diversified multi-path fading simulation accurately and easily by providing an A/D converter, a digital signal processing section and a D/A converter to the simulator so as to analyze the multi-path fading by digital signal processing.

CONSTITUTION: One channel is constituted of a mixer 3, low pass filter 4, A/D converter 5, digital signal processor 6, D/A converter 7, low pass filter 8, mixer 9 and band pass filter 10, and plural channels are provided as required, and the characteristic is controlled entirely by using the controller 2 to which the simulation condition is given from a condition setting device 11. Through the constitution above, a local signal from a local signal generator 1 is mixed with a processing signal by using the mixers 3,9 to implement frequency conversion, and the mixer 3 converts the signal into an intermediate frequency signal within a band of the converter 5, and the mixer 9 decodes conversely the signal into the original RF signal. Thus, the degree of freedom is expanded and the simulation is easily and accurately implemented.



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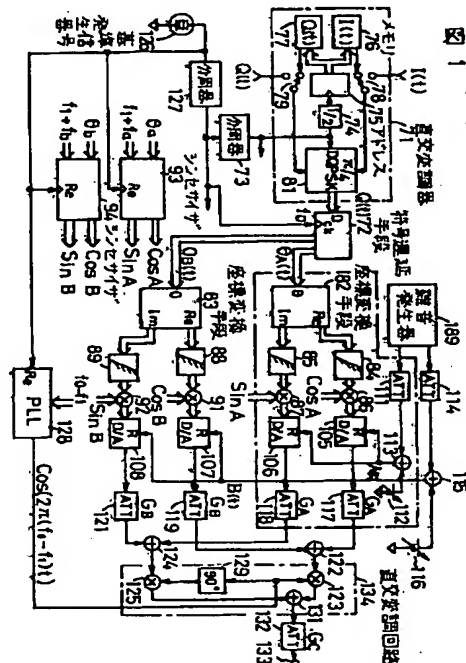
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(54)【発明の名称】 フェージングシュミレータ

(57)【要約】 (修正有)

【目的】温度変動の影響を受けにくく、高周波数の平衡変調器や位相シフタを必要とせず、調整しやすくする。

【構成】フェージングシュミレーションの場合は、符号遅延手段72の同一シフト段から2つの伝送符号 $\theta_a(t)$ と $\theta_b(t)$ を得、又は2つの符号が相関を保つ状態でわずかに遅延量をずらせる。第一電波通路と第二電波通路における各ドブラーシフトは f_a 、 f_b としてそれぞれシンセサイザ93、94に与えられ、2つの電波通路の位相差は設定位相 θ_a 、 θ_b によって決定され、レイリー雑音はA(t)、B(t)で与えられ、減衰量は減衰器117、119によって変化させる。隣接チャネル間の干渉信号を得るには、符号遅延手段より出力される2つの信号 $\theta_a(t)$ と $\theta_b(t)$ とが相関が無い程度に相互に遅延量の差を大きくし、その状態でシンセサイザの設定周波数の一部 f_a と f_b とを十分に離してチャネル間の周波数差を得る。



【特許請求の範囲】

【請求項1】 送信符号のステップ遅延を実現する符号遅延手段と、

位相及び周波数可変な第一、第二デジタルシンセサイザと、

上記符号遅延手段からの2つの符号出力のそれぞれについて第一実部と第一虚部の第二実部と、第二虚部をそれぞれ得る第一、第二座標変換手段と、

上記第一実部及び第一虚部にそれぞれ上記第一シンセサイザの余弦波出力、正弦波出力をそれぞれ掛け算する第一、第二掛け算手段と、

上記第二実部、第二虚部に上記第二シンセサイザの余弦波出力、正弦波出力をそれぞれ掛け算する第三、第四掛け算手段と、

上記第一、第二掛け算手段の出力にそれぞれ雑音を掛け算すると共に、アナログ信号に変換する第一、第二DA変換手段と、

上記第三、第四掛け算手段に上記雑音と異なる雑音をそれぞれ掛け算すると共にアナログ信号に変換する第三、第四DA変換手段と、

上記第一、第三DA変換手段の各出力を加算する第一加算手段と、

上記第二、第四DA変換手段の各出力を加算する第二加算手段と、

上記第一加算手段及び第二加算手段の出力を直交変調する変調手段と、

を具備するフェージングシュミレータ。

【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は、デジタル移動通信システムなどの受信性能を評価するために用いられ、レイリー散乱を受けたり、ドブラーシフトを受けたり、フェージングを受けた状態の信号と同様な信号をリアルタイムで発生するフェージングシュミレータに関する。

【0002】

【従来の技術】図3に従来のフェージングシュミレータを示す。同相信号 $I(t)$ と直交信号 $Q(t)$ とが直交変調器11に加えられ、その変調出力は極座標から直交座標へ変換する座標変換器12においてその実部と虚部とに変換(分割)される。これら変換された実部及び虚部はデジタルの低域通過フィルタ13、14をそれぞれ通じて乗算型のDA変換器15、16にそれぞれ供給される。DA変換器15、16の基準電圧源に可変直流電源17の出力電圧が印加されて直流電圧 V が掛け算される。

【0003】これらDA変換器15、16の出力はそれぞれ掛け算器18、19に供給され、正弦波発振器21からの周波数 f_c の搬送波出力がそのまま掛け算器18に供給されると共に90度移相回路22を通じて掛け算器19に供給され、これら掛け算器18、19の出力は

加算器23で加算され、その加算出力、つまり直交変調出力は掛け算器24において、ランダム雑音発生器25からの雑音が減衰器26で適当なレベルとされた雑音 $A(t)$ と掛け算される。この雑音が掛けられた信号は減衰器27で G_c だけ減衰され、その減衰された出力は可変遅延手段28により t_c だけ遅延されて掛け算器29に供給されると共に移相器31を通じて掛け算器32に供給される。正弦波発振器33より周波数 f_c の信号が掛け算器29に供給されると共に90度移相器34を通じて掛け算器32に供給される。掛け算器29、32の出力は加算器35で加算される。

【0004】一方、加算器23の出力は分岐されて切り替えスイッチ36の固定接点F側を通じて掛け算器37にも供給される。掛け算器37には雑音発生器25からの雑音が減衰器38を通じて雑音 $B(t)$ として与えられている。この掛け算器37の出力は減衰器39により G_c だけ減衰され、さらにその減衰出力は可変遅延手段41により t_c だけ遅延されて掛け算器42へ供給される。周波数 f_c の正弦波を発生する発振器43の出力が掛け算器42に供給されると共に90度移相器44を通じて掛け算器45に供給され、遅延手段41の出力はフェイズシフタ46を通じて掛け算器45も供給される。掛け算器42、45の各出力は加算器47で加算される。加算器35、47の各出力が加算器48により加算され、その加算出力は減衰器49で G_c だけ減衰を受けて出力端子51に出力される。

【0005】また、同相信号 $I'(t)$ 及び直交信号 $Q'(t)$ が直交変調器52において搬送波を直交変調し、その変調出力が座標変換器53において実部と虚部とに変換され取り出され、これら実部及び虚部はデジタルの低域通過フィルタ54、55をそれぞれ通じて乗算型のDA変換器56、57へ供給される。DA変換器56、57には可変電源58より電圧 V が基準電源端子に印加されて V が掛け算される。DA変換器56、57の各出力はそれぞれ掛け算器59、61へ供給され、発振器62からの周波数 f_c の搬送波が掛け算器59に供給されると共に90度移相器63を通じて掛け算器61へ供給される。掛け算器59、61の出力は加算器64で加算され、その加算出力は切り替えスイッチ36の固定接点I側を通じて掛け算器37に供給される。

【0006】移動局と固定局または移動局間の通信においては直接波と反射波とが同時に受信され、しかもその反射波はレベルと位相が変動し、あるいは複数の反射波が主として受信される。このため受信信号はレベル及び位相が変動したものとなる。また移動局と固定局間の相対的移動により受信周波数がいわゆるドブラーシフトにより変動する。これら変動状態を、シュミレーション(フェージングシュミレーション)するには切り替えスイッチ36を固定接点F側とに接続しておく。この時出力端子51に得られる出力信号は次式で表される。

$$\{0007\} G_c \cdot \{G_A \cdot A(t) \cdot \cos\{2\pi(f_A + f_s) \cdot (t - t_A) + \theta_A(t)\} \cdot V_A + G_B \cdot B(t) \cdot \cos\{2\pi(f_B + f_s) \cdot (t - t_B) + \theta_B(t)\} \cdot V_B\}$$

ここでA(t)は電波の第一通路のレイリー散乱であり、B(t)は電波の第二通路のレイリー散乱と等価である。また減衰量G_A、G_Bはそれぞれ第一、第二通路の減衰量である。f_Aが搬送波周波数であり、f_s、f_cがそれぞれ第一、第二通路におけるドブラーシフト周波数である。またθ_A(t)は送信情報である。さらにt_A、t_Bはそれぞれ第一、第二通路の時間遅れである。よってこれらの各部の減衰量あるいは遅延手段28、41の遅延量t_A、t_B、また周波数f_s、f_cなどを変化させることによっていろいろな状態つまり、実際にフェージングを受けた状態をシュミレートすることができる。

【0008】一方隣接チャネル間の干渉をシュミレートするには切り替えスイッチ36を固定接点I側に接続する。この状態における出力端子51の出力は次式で表される。

$$G_c \cdot \{G_A \cdot A(t) \cdot \cos\{2\pi(f_A + f_s) \cdot (t - t_A) + \theta_A(t)\} \cdot V_A + G_B \cdot B(t) \cdot \cos\{2\pi(f_B + f_s) \cdot (t - t_B) + \theta_B(t)\} \cdot V_B\}$$

ここでθ_B(t)はチャネルB側の送信情報である。f_BはチャネルB側の搬送波周波数である。この場合隣接チャネル間においては搬送波周波数がf_A + f_sとf_B + f_s間の干渉となり且つこれらの時間ないし位相は遅延手段28、41によって調整され、その周波数差はf_s、f_c、f_A、f_Bによって変更され、レベルはG_A、G_Bで変更される。

【0009】

【発明が解決しようとする課題】従来においては、2つの通路差を変更するため可変遅延手段28、41が用いられているが、この遅延時間t_A、t_Bを得るには通常、線路いわゆるケーブルの遅延時間を利用しているため温度変動にしたがって遅延時間が変化し、また周波数によって遅延歪みが生じ、さらに高い分解能で広い範囲によって遅延時間を変化することが難しい。

【0010】また多数の高周波数の平衡変調器つまり掛け算器18、19、24、29、32、37、42、45、59、61を使用しており、さらに多くの高周波の位相シフタを使用しているため、周波数に対する調整が難しい。しかも2つの系統が用いられ構成が複雑となっていた。

【0011】

【課題を解決するための手段】この発明によれば、符号遅延手段から送信符号がステップ的に遅延され、その2つの遅延出力の各符号について第一実部と第一虚部、第二実部と第二虚部が第一、第二座標交換手段により交換

され、これら第一実部、第一虚部は第一デジタルシンセサイザからの余弦波出力及び正弦波出力とそれぞれ第一、第二掛け算手段によって掛け算され、またこれら第一、第二掛け算手段の出力はそれぞれ第一、第二乗算型DA変換手段によって雑音が掛けられると共にアナログ信号に変換される。一方第二実部、第二虚部は第二デジタルシンセサイザからの余弦波出力と正弦波出力がそれぞれ第三、第四掛け算手段によって掛け算され、これら第三、第四掛け算出力は第三、第四乗算型DA変換手段によって、上記とことなる雑音が掛け算されると共にアナログ信号に変換される。第一、第三DA変換手段の出力が第一加算手段で加算され、第二、第三、第四DA変換手段の出力は第二加算手段で加算され、これら第一、第二加算手段の出力が直交変調手段で直交変調される。

【0012】

【実施例】図1にこの発明の実施例を示す。直交変調器71からの送信情報θ(t)は、符号遅延手段72に供給されてその符号単位即ちステップ的遅延が行われる。

符号遅延手段72は例えばシフトレジスタやFIFOメモリなどが用いられる。また直交変調器71としては、データ発生用クロック発生器73よりのデータ発生用クロックが分周器74で1/2に分周され、その分周出力がアドレスカウンタ75で計数され、そのアドレスカウンタ75の計数値をアドレスとして同相メモリ76、直交用メモリ77がそれぞれ読みだされて同相信号I(t)と直交信号Q(t)とが出力される。これら両出力がそれぞれ切り替えスイッチ78、79を通じて変調器81へ供給され搬送波長、例えばπ/4DQPSK変調する。スイッチ78、79は外部からの同相信号及び直交信号を入力する場合に切り替えられる。

【0013】符号遅延手段72よりそれぞれ符号単位でことなる遅延が与えられた、あるいは同一の遅延が与えられた信号が出力される。符号遅延手段72が例えばシフトレジスタの場合は異なるタップ(シフト段)からの出力あるいは同一タップ(シフト段)からの出力がそれぞれ符号送信情報θ_A(t)と、θ_B(t)として取り出され、座標変換手段82、83へ供給される。座標変換手段82、83において各入力符号はそれぞれ極座標、直交座標の交換が行われて実部と虚部がそれぞれ出力される。座標変換手段82からの実部及び虚部はそれぞれ必要に応じてFIR形デジタル低域通過フィルタ84、85を通じて乗算器86、87へ供給される。また座標変換手段83よりの実部及び虚部はそれぞれ必要に応じてFIR形デジタル低域通過フィルタ88、89を通じて乗算器91、92に供給される。

【0014】一方デジタルシンセサイザ93、94が設けられる。デジタルシンセサイザ93、94はそれぞれ位相及び周波数を変化することができるもので、例えば図2Aに示すように構成される。即ちトル型のフ

リップフロップ95からの周波数 f_r が $1/2$ とされた一方の出力によりラッチ回路96に加算器97の出力をラッチする。加算器97はラッチ回路96の出力と周波数データ k_r とを加算する。またラッチ回路96の出力は位相データ k_θ と加算回路98で加算され、その出力は、移相回路99において0度の位相または90度の位相シフトが与えられて、正弦波メモリ101へ読み出しアドレスとして供給される。正弦波メモリ101には正弦波形の各サンプル点のレベルが記憶されており、その読み出されたデジタルの正弦波信号は、ラッチ回路26
10 に対するラッチ指令によってラッチ回路102にラッチされ、またこのラッチ指令に対して180度位相がずれた信号によってラッチ回路103にラッチされる。ラッチ回路102の出力がデジタル正弦波出力となり、ラッチ回路103の出力がラッチ回路26に対するラッチと同時にラッチ回路104にラッチされ、ラッチ回路104からデジタルの余弦波出力が得られる。周波数データ k_r が周波数 $f_r/2$ のクロックごとに累積加算されるため、周波数データ k_r が大きいほど周波数が高くなり、周波数データ k_r が小さいほど周波数は低くなる。移相回路99はそのまま出力するか、90度位相をずらして出力するものであるから図2Bに示すように、その入力データの最上位のビットと次のビットをそのまま通過するか、それらを排他的論理和を取ったものを最上位ビットとし、最上位から2番目のビットを反転したものを最上位から2番目のビットとして出力するかの切り替えを行えばよい。このようにして周波数が $f_r \times k_r / 2^{11}$ 、位相 θ が $2\pi \times k_\theta / 2^4$ の正弦波出力と余弦波出力とが得られる。 f_r はフリップフロップ95を駆動するクロックの周波数である。

【0015】図1の説明に戻って、シンセサイザ93に対して周波数 $f_1 + f_a$ が設定され、位相 θ_a が設定され、これにより余弦波出力 $\cos\{2\pi(f_1 + f_a)t + \theta_a\}$ が出力されて乗算器86に供給され、また正弦波出力 $\sin\{2\pi(f_1 + f_a)t + \theta_a\}$ が出力されて乗算器87に供給される。一方シンセサイザ94に対しては周波数 $f_1 + f_b$ が設定され、位相 θ_b が出力され、その余弦波出力 $\cos\{2\pi(f_1 + f_b)t + \theta_b\}$ が乗算器91に供給され、正弦波出力 $\sin\{2\pi(f_1 + f_b)t + \theta_b\}$ が乗算器92に供給される。乗算器86、87の各出力はそれぞれ乗算型DA変換器105、106に供給され、また乗算器91、92の各出力はそれぞれ乗算型DA変換器107、108に供給される。一方ランダム雑音発生器109よりランダム雑音が発生され、その雑音は必要に応じて減衰器111にて減衰された後、可変直流電源112よりの直流電圧と加算回路113で加算され、その加算回路113の出力がレイリー雑音A(t)として乗算型DA変換器105、106の各基準電源端子に供給されてその入力デジタル信号と掛け算されると共に、そのデ

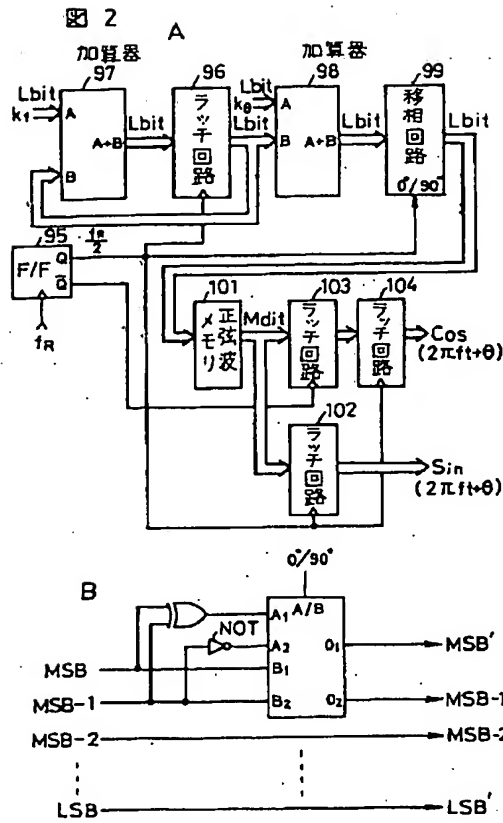
ジタル信号がアナログ信号に変換される。同様に雑音発生器109からの雑音が減衰器114を通じて加算器115に供給されて可変直流電源116の出力直流電圧とが加算され、加算器115からの出力がレイリー雑音B(t)として乗算器DA変換器107、108の基準電源端子に供給されて、その入力デジタル信号に対して掛け算されると共にそのデジタル信号をアナログ信号に変換される。

【0016】DA変換器105、106の各出力はそれぞれ減衰器117、118においてそれぞれ G_a ずつ減衰され、またDA変換器107、108よりの各出力は減衰器119、121においてそれぞれ G_b だけ減衰される。減衰器117、119の出力は加算器122において加算されて乗算器123に供給され、また減衰器118、121の各出力は加算器124で加算されて乗算器125に供給される。

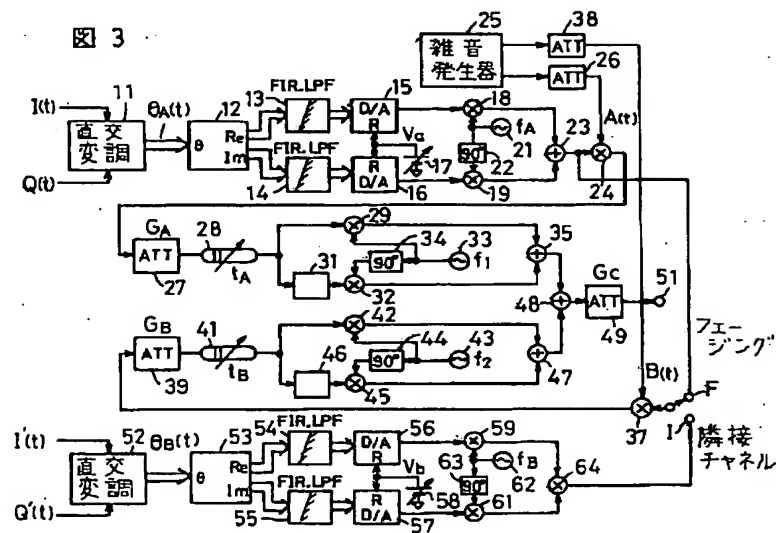
【0017】基準信号発生器126よりの信号は周波数 f_r であってシンセサイザ93、94にそれぞれクロックとして供給されると共に、その出力は分周器127により整数分の1に分周されてデータ発生用クロック発生器27に供給されると共に、符号遅延手段72に対するシフトクロックとして供給され、その他のデジタル処理のためのクロックとして各部に供給される。さらに基準信号発生器126の出力は位相ロックループ(PLL)128に基準信号として供給され、そのPLL128には搬送波周波数 $f_c - f_1$ が設定入力され、基準信号と同期した周波数 $f_c - f_1$ の信号 $\cos\{2\pi(f_c - f_1)t\}$ が出力され、これが搬送波信号として乗算器123に供給されると共に90度移相器129を通じて乗算器125に供給される。乗算器123、125の出力は加算器131で加算され、その加算出力は減衰器132にて減衰されて出力端子133に出力される。乗算器123、125、移相器129、加算器131は直交変調回路134を構成している。またPLL128の出力搬送波周波数を $f_c - f_1$ とするのは出力端子133の出力信号の搬送波周波数 f_c を増加したり減少する必要があり、つまりシンセサイザ93、94において負の周波数を発生することができないから、 f_1 だけ高い周波数として、それに対して正、負の周波数 f_a 、 f_b を自由に選ぶことができ、これによりその直交変調回路13における出力搬送波の周波数を中心 f_c に対し、正にも負にも f_a 、 f_b だけ変化することができる。

【0018】この構成においては、符号遅延手段72にシフトレジスタを使用し、そのシフト周波数を f_d とし、出力が取り出されるシフト段を n_a 、 n_b とすると、座標変換手段82、83に供給される符号情報はそれぞれ $\theta_a(t) = \theta(t - n_a/f_d)$ 、 $\theta_b(t) = \theta(t - n_b/f_d)$ となる。よって端子133により出力される信号は次のようになる。

【図2】



【図3】



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CLAIMS

[Claim(s)]

[Claim 1] A sign delay means to realize step delay of a transmitting sign, and the strange first with good phase and frequency and the second digital synthesizer, About each of two sign outputs from the above-mentioned sign delay means, the first real part and the second real part of the first imaginary part, A first and second coordinate transformation means to obtain the second imaginary part, respectively, and a first and second multiplication means to multiply the first real part of the above, and the first imaginary part by the cosine wave output of the first synthesizer of the above, and the sinusoidal output, respectively, While multiplying the output of a third and fourth multiplication means to multiply the second real part of the above, and the second imaginary part by the cosine wave output of the second synthesizer of the above, and the sinusoidal output, respectively, and the above-mentioned first and second multiplication means by the noise, respectively The first changed into an analog signal, the second DA translation means, and a third and fourth DA translation means to change into an analog signal while multiplying the above-mentioned third and fourth multiplication means by the above-mentioned noise and different noise, respectively, The phasing simulator possessing a first addition means to add each output of the third DA translation means for a start [above-mentioned], a second addition means to add each output of the above-mentioned second and fourth DA translation means, and the modulation means that carries out quadrature modulation of the output of the above-mentioned first addition means and the second addition means.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention is used in order to evaluate receiving engine performance, such as digital migration communication system, and receive Rayleigh scattering, a Doppler shift is received, or it relates phasing to the phasing simulator generated on real time in the signal of a carrier beam condition, and the same signal.

[0002]

[Description of the Prior Art] The conventional phasing simulator is shown in drawing 3. In-phase signal $I(t)$ and rectangular signal $Q(t)$ is added to the quadrature modulation machine 11, and the modulation output is changed into the real part and imaginary part in the coordinate transformation machine 12 changed into rectangular coordinates from a polar coordinate (division). The real part and imaginary part which were these-changed are supplied to DA converters 15 and 16 of a multiplication mold respectively through the digital low pass filters 13 and 14, respectively. The output voltage of adjustable DC power supply 17 is impressed to the source of reference voltage of DA converters 15 and 16, and it is direct current voltage V_A . It multiplies.

[0003] The output of these DA converters 15 and 16 is supplied to multipliers 18 and 19, respectively. Frequency f_A from a sine wave oscillator 21 While a subcarrier output is supplied to a multiplier 18 as it is, a multiplier 19 is supplied through a phase-shifting circuit 22 90 degrees. The output of these multipliers 18 and 19 is added with an adder 23, and it multiplies by the addition output, i.e., a quadrature modulation output, in a multiplier 24 with noise $A(t)$ by which the noise from the random noise generator 25 was made suitable level with the attenuator 26. the signal with which this noise was imposed -- an attenuator 27 -- G_A only -- it decreases -- having -- that decreased output -- the adjustable delay means 28 -- t_A only -- while being delayed and supplying a multiplier 29, a multiplier 32 is supplied through a phase shifter 31. It is a frequency f_1 from the sine oscillator 33. While a signal is supplied to a multiplier 29, a multiplier 32 is supplied through a phase shifter 34 90 degrees. The output of multipliers 29 and 32 is added with an adder 35.

[0004] On the other hand, the output of an adder 23 branches and is supplied also to a multiplier 37 through the stationary-contact F side of a changeover switch 36. The noise from a noise generator 25 is given to the multiplier 37 as noise $B(t)$ through the attenuator 38. the output of this multiplier 37 -- an attenuator 39 -- G_B only -- it decreases -- having -- further -- that attenuation output -- the adjustable delay means 41 -- t_B only -- it is delayed and a multiplier 42 is supplied. Frequency f_2 While the output of the oscillator 43 which generates a sine wave is supplied to a multiplier 42, a multiplier 45 is supplied through a phase shifter 44 90 degrees, and as for the output of the delay means 41, a multiplier 45 is also supplied through the phase shifter 46. Each output of multipliers 42 and 45 is added with an adder 47. each output of adders 35 and 47 adds with an adder 48 -- having -- the addition output -- an attenuator 49 -- G_C only -- in response to attenuation, it is outputted to an output terminal 51.

[0005] Moreover, in-phase signal $I'(t)$ and rectangular signal $Q'(t)$ carry out quadrature modulation of the subcarrier in the quadrature modulation machine 52, in the coordinate

transformation machine 53, the modulation output is changed into real part and imaginary part, and is taken out, and these real part and imaginary part are supplied to DA converters 56 and 57 of a multiplication mold respectively through the digital low pass filters 54 and 55. In DA converters 56 and 57, it is an electrical potential difference VB from the adjustable power source 58. It is impressed by the criteria power supply terminal, and is VB. It multiplies. Multipliers 59 and 61 are supplied and each output of DA converters 56 and 57 is the frequency fB from an oscillator 62, respectively. While a subcarrier is supplied to a multiplier 59, a multiplier 61 is supplied through a phase shifter 63 90 degrees. The output of multipliers 59 and 61 is added with an adder 64, and the addition output is supplied to a multiplier 37 through the stationary-contact I side of a changeover switch 36.

[0006] In the communication link between a mobile station, a fixed station, or a mobile station, a direct wave and a reflected wave are received simultaneously, and moreover, as for the reflected wave, level and a phase are changed, or two or more reflected waves are mainly received. For this reason, an input signal becomes that to which level and a phase were changed. Moreover, received frequency is changed by the so-called Doppler shift by the relative movement between a mobile station and a fixed station. For carrying out the simulation (phasing simulation) of these fluctuation condition, the changeover switch 36 is connected to the stationary-contact F side. The output signal acquired by the output terminal 51 at this time is expressed with a degree type.

[0007]
$$GC - [\text{---} GA - A \text{---} (\text{---} t \text{---}) - \cos \text{---} \{ \text{---} \text{two} \text{---} \pi (fA+f1) - (t-tA) \text{---} + \text{---} \theta_A \text{---} A \text{---} (\text{---} t \text{---}) \text{---} \} - VA \text{---} + \text{---} GB - B \text{---} (\text{---} t \text{---}) - \cos \text{---} \{ \text{---} \text{two} \text{---} \pi (fA+f2) - (t-tB) \text{---} + \text{---} \theta_A \text{---} A \text{---} (\text{---} t \text{---}) \text{---} \} - VA \text{---}]$$

A (t) is Rayleigh scattering of the first path of an electric wave, and its B (t) is equivalent to Rayleigh scattering of the second path of an electric wave here. Moreover, the magnitude of attenuation GA and GB It is the magnitude of attenuation of the second path for a start, respectively. fA It is carrier frequency and is f1 and f2. It is a Doppler shift frequency in the second path for a start, respectively. Moreover, θ_A (t) is transmit information. Furthermore, they are tA and tB. It is the time lag of the second path for a start, respectively. therefore, the magnitude of attenuation of these each part or the amount tA of delay of the delay means 28 and 41, and tB again -- a frequency f1 and f2 etc. -- making it change -- various conditions -- that is, a carrier beam condition can be actually simulated for phasing.

[0008] For, simulating interference between adjacent channels on the other hand, a changeover switch 36 is connected to a stationary-contact I side. The output of the output terminal 51 in this condition is expressed with a degree type.

$$GC - [\text{---} GA - A \text{---} (\text{---} t \text{---}) - \cos \text{---} \{ \text{---} \text{two} \text{---} \pi (fA+f1) - (t-tA) \text{---} + \text{---} \theta_A \text{---} A \text{---} (\text{---} t \text{---}) \text{---} \} - VA \text{---} + \text{---} GB - B \text{---} (\text{---} t \text{---}) - \cos \text{---} \{ \text{---} \text{two} \text{---} \pi (fB+f2) - (t-tB) \text{---} + \text{---} \theta_B \text{---} B \text{---} (\text{---} t \text{---}) \text{---} \} - VB \text{---}]$$

It is θ_B here. (t) is the transmit information by the side of Channel B. fB It is the carrier frequency by the side of Channel B. In this case, it sets between adjacent channels and carrier frequency is fA+f1. fB+f2 It becomes interference of a between, and these time amount thru/or phases is adjusted by the delay means 28 and 41, and that frequency difference is f1, f2, fA, and fB. It is changed and level is GA and GB. It is changed.

[0009]

[Problem(s) to be Solved by the Invention] Although the adjustable delay means 28 and 41 are used in the former in order to change two path differences, they are this time delay tA and tB. It is difficult for a time delay to change according to temperature fluctuation, since the time delay of a line ***** cable is usually used for obtaining, and for delay distortion to arise with a frequency and to change a time delay with large range with still higher resolution.

[0010] Moreover, since it is used, many the balanced modulators 18, 19, 24, 29, 32, 37, 42, 45, 59, and 61, i.e., the multipliers, of high frequency, and the phase shifter of much more RFs is used, the adjustment to a frequency is difficult. And two systems were used and the configuration was complicated.

[0011]

[Means for Solving the Problem] According to this invention, a transmitting sign is delayed from

a sign delay means in step. The first real part, the first imaginary part and the second real part, and the second imaginary part about each sign of the two delay outputs. The first, It is changed by the second coordinate operator stage. These first real part and the first imaginary part, respectively with the cosine wave output from the first digital synthesizer, and a sinusoidal output. The first, It multiplies with the second multiplication means, and for a start [these], the output of the second multiplication means is changed into an analog signal, respectively while a noise is imposed by the second multiplication mold DA translation means for a start. on the other hand, the cosine wave output and the sinusoidal output from the second digital synthesizer multiply by the second real part and the second imaginary part with the third and fourth multiplication means, respectively -- having -- these third and fourth multiplication output -- the third and fourth multiplication mold DA translation means -- the above -- things -- it is changed into an analog signal while a noise multiplies. For a start, the output of the third DA translation means is added with the first addition means, the output of the second, third, and fourth DA translation means is added with the second addition means, and quadrature modulation of the output of the second addition means is carried out with a quadrature modulation means for a start [these].

[0012]

[Example] The example of this invention is shown in drawing 1. Transmit information [from the quadrature modulation machine 71] $\theta(t)$ is supplied to the sign delay means 72, and the sign unit, i.e., step-delay, is performed. As for the sign delay means 72, a shift register, a FIFO memory, etc. are used. Moreover, as a quadrature modulation machine 71, dividing of the clock for data generating from the clock generation machine 73 for data generating is carried out to one half with a counting-down circuit 74, counting of the dividing output is carried out with an address counter 75, the memory 76 for inphases and the memory 77 for a rectangular cross are read considering the enumerated data of the address counter 75 as the address, respectively, and in-phase signal $I(t)$ and rectangular signal $Q(t)$ is outputted. both [these] outputs supply a modulator 81 through changeover switches 78 and 79, respectively -- having -- subcarrier length -- for example, a $\pi/4$ -Differential-QPSK modulation is carried out. Switches 78 and 79 are changed when inputting the in-phase signal and the rectangular signal from the outside.

[0013] the sign delay means 72 -- respectively -- a sign unit -- things -- delay was given or the signal with which the same delay was given is outputted. The output from a tap (shift stage) which is different when the sign delay means 72 is a shift register, or the output from the same tap (shift stage) is sign transmit information θ_A , respectively. (t) and θ_B It is taken out as (t) and the coordinate transformation means 82 and 83 are supplied. In the coordinate transformation means 82 and 83, conversion of a polar coordinate and rectangular coordinates is performed and, as for each input sign, real part and imaginary part are outputted, respectively. The real part and imaginary part from the coordinate transformation means 82 are supplied to multipliers 86 and 87 through the FIR form digital low pass filters 84 and 85 if needed, respectively. Moreover, the real part and imaginary part from the coordinate transformation means 83 are supplied to multipliers 91 and 92 through the FIR form digital low pass filters 88 and 89 if needed, respectively.

[0014] On the other hand, the digital synthesizers 93 and 94 are formed. The digital synthesizers 93 and 94 are constituted, as it can change and a phase and a frequency are shown in drawing 2 A, respectively. Namely, frequency f_R from the flip-flop 95 of a toggle mold While was set to one half and the output of an adder 97 is latched to a latch circuit 96 with an output. An adder 97 is the output and the frequency data k_f of a latch circuit 96. It adds. Moreover, the output of a latch circuit 96 is added in phase data $k\theta$ and an adder circuit 98, and in a phase-shifting circuit 99, the phase of 0 times or the phase shift of 90 degrees is given, and the output is read to the sinusoidal memory 101, and is supplied as the address. It is latched to a latch circuit 103 by the signal with which the level of each sample point of a sinusoidal form is memorized by the sinusoidal memory 101, and that digital sinusoidal signal by which reading appearance was carried out was latched to the latch circuit 102 by the latch command to a latch circuit 26, and the phase shifted about 180 degrees to this latch command. The output of a latch circuit 102 turns into a digital sine wave output, the output of a latch circuit 103 is latched to the latch and

coincidence to a latch circuit 26 by the latch circuit 104, and a digital cosine wave output is obtained from a latch circuit 104. Frequency data k_f Since accumulation is carried out every clock of frequency $f_R / 2$, it is the frequency data k_f . A frequency becomes high, so that it is large, and it is the frequency data k_f . A frequency becomes low, so that it is small. What is necessary is just to change whether the most significant bit of the input data and the following bit are passed as it is, or what made what took the exclusive OR for them the most significant bit, and reversed the 2nd bit from the most significant is outputted as 2nd bit from the most significant, as shown in drawing 2 B since a phase-shifting circuit 99 is outputted as it is or a phase is shifted and outputted about 90 degrees. Thus, for a frequency, $f_R \times k_f / 2L + 1$ and a phase θ are $2\pi k_f \theta / 2L$. A sinusoidal output and a cosine wave output are obtained. f_R It is the frequency of the clock which drives a flip-flop 95.

[0015] It returns to explanation of drawing 1, frequency $f_1 + f_a$ is set up to a synthesizer 93, phase θ_a is set up, the cosine wave output $\cos \{2\pi(f_1 + f_a) t + \theta_a\}$ is outputted by this, a multiplier 86 is supplied, and the sinusoidal output $\sin \{2\pi(f_1 + f_a) t + \theta_a\}$ is outputted, and a multiplier 87 is supplied. On the other hand to a synthesizer 94, frequency $f_1 + f_b$ is set up, phase θ_b is outputted, the cosine wave output $\cos \{2\pi(f_1 + f_b) t + \theta_b\}$ is supplied to a multiplier 91, and the sinusoidal output $\sin \{2\pi(f_1 + f_b) t + \theta_b\}$ is supplied to a multiplier 92. Each output of multipliers 86 and 87 is supplied to multiplication mold DA converter 105, 106, respectively, and each output of multipliers 91 and 92 is supplied to multiplication mold DA converter 107, 108, respectively. On the other hand, random noise is generated from the random noise generator 109, and after decreasing the noise with an attenuator 111 if needed, while being added in the direct current voltage and the adder circuit 113 from adjustable DC power supply 112, supplying the output of the adder circuit 113 to each criteria power supply terminal of multiplication mold DA converter 105, 106 as Rayleigh noise $A(t)$ and multiplying by it with the input digital signal, the digital signal is changed into an analog signal. The noise from a noise generator 109 is similarly supplied to an adder 115 through an attenuator 114, the output direct current voltage of adjustable DC power supply 116 is added, the output from an adder 115 is supplied to the criteria power supply terminal of multiplier DA converter 107, 108 as Rayleigh noise $B(t)$, and while multiplying to the input digital signal, the digital signal is changed by the analog signal.

[0016] each output of DA converter 105, 106 -- respectively -- an attenuator 117, 118 -- setting -- respectively -- every $[G_a]$ -- it decreases -- having -- moreover, each output from DA converter 107, 108 -- an attenuator 119, 121 -- setting -- respectively -- G_b only -- it decreases. The output of an attenuator 117, 119 is added in an adder 122, and is supplied to a multiplier 123, and each output of an attenuator 118, 121 is added with an adder 124, and is supplied to a multiplier 125.

[0017] the signal from the reference signal generator 126 -- frequency f_R it is -- while synthesizers 93 and 94 are supplied as a clock, respectively, dividing of the output is carried out to 1 for an integer by the counting-down circuit 127, while the clock generation machine 27 for data generating is supplied, it is supplied as a shift clock to the sign delay means 72, and each part is supplied as a clock for other digital processings. Furthermore, the output of the reference signal generator 126 is supplied to a phase locked loop (PLL) 128 as a reference signal. In the PLL 128, it is carrier frequency $f_0 - f_1$. A setting-out input is carried out. Frequency $f_0 - f_1$ which is synchronized with the reference signal $\text{Signal} \cos \{2\pi(f_0 - f_1) - t\}$ is outputted, and while this is supplied to a multiplier 123 as a carrier signal, a multiplier 125 is supplied through a phase shifter 129 90 degrees. The output of a multiplier 123, 125 is added with an adder 131, and the addition output is decreased with an attenuator 132, and is outputted to an output terminal 133. The multiplier 123, 125, the phase shifter 129, and the adder 131 constitute the quadrature modulation circuit 134. Moreover, it is the output carrier frequency of PLL 128 $f_0 - f_1$ What is carried out is the carrier frequency f_0 of the output signal of an output terminal 133. It is necessary to increase or to decrease. that is, -- since a negative frequency cannot be generated in synthesizers 93 and 94 -- f_1 only -- as a high frequency It is a core f_0 about the frequency of an output subcarrier [in / by this / forward and the negative frequencies f_a and f_b can be freely chosen to it, and / the quadrature modulation circuit 13]. It can receive and only f_a and f_b can

change to forward and negative.

[0018] In this configuration, a shift register is used for the sign delay means 72, and it is fd about that shift frequency. If it carries out and the shift stage where an output is taken out is set to na and nb, the sign information supplied to the coordinate transformation means 82 and 83 is thetaA, respectively. $\theta(t) = \theta(t - na/fd)$ and thetaB It is set to $\theta(t) = \theta(t - nb/fd)$. Therefore, the signal outputted with a terminal 133 is as follows.

[0019] $G_c = [2\pi(f_0 + f_a) \text{ and } G_a - A(t) \text{ and } \cos\{t + \theta_a + \theta(t - na/fd)\} + G_b - B(t) \text{ and } \cos\{2\pi(f_0 + f_b) \text{ and } t + \theta_b + \theta(t - nb/fd)\}]$

In the case of a phasing simulation, it is two modulation-codes [the same shift stage in the sign election means 72 to] thetaA. $\theta(t)$ and thetaB $\theta(t)$ is obtained or it is modulation-code thetaA. $\theta(t)$ and thetaB $\theta(t)$ shifts the amount of delay only in the condition of maintaining correlation.

Rayleigh scattering over the path of two electric waves is given as A $\theta(t)$ and B $\theta(t)$, and a value with each Doppler shift respectively small as fa and fb in the first electric-wave path and second electric-wave path is given. The phase contrast of the two electric-wave paths is determined by setting-out phase thetaa in the digital synthesizers 93 and 94, and thetab, the Rayleigh noise is given by A $\theta(t)$ and B $\theta(t)$, and the magnitude of attenuation is changed by the attenuator 117,119. The time delay of the first electric-wave path is given by $\{(na/fd) - \theta_a / 2\pi(f_0 + f_a)\}$, and the time lag of the second electric-wave path is given by $\{(nb/fd) - \theta_b / 2\pi(f_0 + f_b)\}$. The signal with which each part was controlled and the phasing effectiveness was given like the conventional technique can be acquired by doing in this way.

[0020] Moreover, two signals thetaA which sets for the sign delay means 27 and is outputted more when acquiring the interference signal between adjacent channels $\theta(t)$ and thetaB In order that $\theta(t)$ may make the difference of the amount of delay size mutually at extent without correlation and may obtain the delta frequency between channels in the condition, a part of setting-out frequency fa and fb of synthesizers 93 and 94 is detached enough mutually. Also in this case, the simulation of the interference signal between adjacent channels can be carried out as usual.

[0021] In ***, the simulation of multi-pass phasing and the interference simulation between other a large number channels can be performed by preparing two or more groups of the coordinate transformation means 82, filters 84 and 85, multipliers 86 and 87, DA converter 105,106, an attenuator 111, an adder 113, an attenuator 117,118, and a power source 112. Moreover, in ***, although the phasing simulation about a pai-fourth-Differential-QPSK modulating signal was performed, the simulation of phasing to other communication modes or interference between adjacent channels can also be performed by changing a modulator 71.

[0022]

[Effect of the Invention] In order to make in digital one using the difference of the delay [according to / like / this invention / in / for the difference of two paths, or the difference of the signal path of adjacent channel interference / the sign delay means 72] which stated above, the difference of the setting-out phase in frequency synthesizers 93 and 94, etc., Since the delay line is not used like before, it is not influenced by fluctuation of ambient temperature, and it reaches far and wide and it is [it is stable to temperature or frequency change and] possible continuous and to perform a transit delay simulation without distortion. Moreover, since processing of Rayleigh scattering or a Doppler shift is realized in digital one on the comparatively low frequency, the balanced modulator and phase shifter in a high frequency are good only only in the quadrature modulation circuit 134 in a tail end, and, therefore, the adjustment to a frequency is easy for them.

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TECHNICAL FIELD

[Industrial Application] This invention is used in order to evaluate receiving engine performance, such as digital migration communication system, and receive Rayleigh scattering, a Doppler shift is received, or it relates phasing to the phasing simulator generated on real time in the signal of a carrier beam condition, and the same signal.

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PRIOR ART

[Description of the Prior Art] The conventional phasing simulator is shown in drawing 3. In-phase signal $I(t)$ and rectangular signal $Q(t)$ is added to the quadrature modulation machine 11, and the modulation output is changed into the real part and imaginary part in the coordinate transformation machine 12 changed into rectangular coordinates from a polar coordinate (division). The real part and imaginary part which were these-changed are supplied to DA converters 15 and 16 of a multiplication mold respectively through the digital low pass filters 13 and 14, respectively. The output voltage of adjustable DC power supply 17 is impressed to the source of reference voltage of DA converters 15 and 16, and it is direct current voltage V_A . It multiplies.

[0003] The output of these DA converters 15 and 16 is supplied to multipliers 18 and 19, respectively. Frequency f_A from a sine wave oscillator 21 While a subcarrier output is supplied to a multiplier 18 as it is, a multiplier 19 is supplied through a phase-shifting circuit 22 90 degrees. The output of these multipliers 18 and 19 is added with an adder 23, and it multiplies by the addition output, i.e., a quadrature modulation output, in a multiplier 24 with noise $A(t)$ by which the noise from the random noise generator 25 was made suitable level with the attenuator 26. the signal with which this noise was imposed -- an attenuator 27 -- G_A only -- it decreases -- having -- that decreased output -- the adjustable delay means 28 -- t_A only -- while being delayed and supplying a multiplier 29, a multiplier 32 is supplied through a phase shifter 31. It is a frequency f_1 from the sine oscillator 33. While a signal is supplied to a multiplier 29, a multiplier 32 is supplied through a phase shifter 34 90 degrees. The output of multipliers 29 and 32 is added with an adder 35.

[0004] On the other hand, the output of an adder 23 branches and is supplied also to a multiplier 37 through the stationary-contact F side of a changeover switch 36. The noise from a noise generator 25 is given to the multiplier 37 as noise $B(t)$ through the attenuator 38. the output of this multiplier 37 -- an attenuator 39 -- G_B only -- it decreases -- having -- further -- that attenuation output -- the adjustable delay means 41 -- t_B only -- it is delayed and a multiplier 42 is supplied. Frequency f_2 While the output of the oscillator 43 which generates a sine wave is supplied to a multiplier 42, a multiplier 45 is supplied through a phase shifter 44 90 degrees, and as for the output of the delay means 41, a multiplier 45 is also supplied through the phase shifter 46. Each output of multipliers 42 and 45 is added with an adder 47. each output of adders 35 and 47 adds with an adder 48 -- having -- the addition output -- an attenuator 49 -- G_C only -- in response to attenuation, it is outputted to an output terminal 51.

[0005] Moreover, in-phase signal $I'(t)$ and rectangular signal $Q'(t)$ carry out quadrature modulation of the subcarrier in the quadrature modulation machine 52, in the coordinate transformation machine 53, the modulation output is changed into real part and imaginary part, and is taken out, and these real part and imaginary part are supplied to DA converters 56 and 57 of a multiplication mold respectively through the digital low pass filters 54 and 55. In DA converters 56 and 57, it is an electrical potential difference V_B from the adjustable power source 58. It is impressed by the criteria power supply terminal, and is V_B . It multiplies. Multipliers 59 and 61 are supplied and each output of DA converters 56 and 57 is the frequency f_B from an oscillator 62, respectively. While a subcarrier is supplied to a multiplier 59, a multiplier 61 is

supplied through a phase shifter 63 90 degrees. The output of multipliers 59 and 61 is added with an adder 64, and the addition output is supplied to a multiplier 37 through the stationary-contact I side of a changeover switch 36.

[0006] In the communication link between a mobile station, a fixed station, or a mobile station, a direct wave and a reflected wave are received simultaneously, and moreover, as for the reflected wave, level and a phase are changed, or two or more reflected waves are mainly received. For this reason, an input signal becomes that to which level and a phase were changed. Moreover, received frequency is changed by the so-called Doppler shift by the relative movement between a mobile station and a fixed station. For carrying out the simulation (phasing simulation) of these fluctuation condition, the changeover switch 36 is connected to the stationary-contact F side. The output signal acquired by the output terminal 51 at this time is expressed with a degree type.

[0007]
$$GC = [GA - A \cos \{2\pi (f_A + f_1)(t - t_A) + \theta_A - (t - t_A)\} - VA + GB - B \cos \{2\pi (f_A + f_2)(t - t_B) + \theta_A - (t - t_B)\} - VA]$$

A (t) is Rayleigh scattering of the first path of an electric wave, and its B (t) is equivalent to Rayleigh scattering of the second path of an electric wave here. Moreover, the magnitude of attenuation GA and GB It is the magnitude of attenuation of the second path for a start, respectively. fA It is carrier frequency and is f1 and f2. It is a Doppler shift frequency in the second path for a start, respectively. Moreover, thetaA (t) is transmit information. Furthermore, they are tA and tB. It is the time lag of the second path for a start, respectively. therefore, the magnitude of attenuation of these each part or the amount tA of delay of the delay means 28 and 41, and tB again -- a frequency f1 and f2 etc. -- making it change -- various conditions -- that is, a carrier beam condition can be actually simulated for phasing.

[0008] For, simulating interference between adjacent channels on the other hand, a changeover switch 36 is connected to a stationary-contact I side. The output of the output terminal 51 in this condition is expressed with a degree type.

$$GC = [GA - A \cos \{2\pi (f_A + f_1)(t - t_A) + \theta_A - (t - t_A)\} - VA + GB - B \cos \{2\pi (f_B + f_2)(t - t_B) + \theta_B - (t - t_B)\} - VB]$$

It is thetaB here. (t) is the transmit information by the side of Channel B. fB It is the carrier frequency by the side of Channel B. In this case, it sets between adjacent channels and carrier frequency is fA+f1. fB+f2 It becomes interference of a between, and these time amount thru/or phases is adjusted by the delay means 28 and 41, and that frequency difference is f1, f2, fA, and fB. It is changed and level is GA and GB. It is changed.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] In order to make in digital one using the difference of the delay [according to / like / this invention / in / for the difference of two paths, or the difference of the signal path of adjacent channel interference / the sign delay means 72] which stated above, the difference of the setting-out phase in frequency synthesizers 93 and 94, etc., Since the delay line is not used like before, it is not influenced by fluctuation of ambient temperature, and it reaches far and wide and it is [it is stable to temperature or frequency change and] possible continuous and to perform a transit delay simulation without distortion. Moreover, since processing of Rayleigh scattering or a Doppler shift is realized in digital one on the comparatively low frequency, the balanced modulator and phase shifter in a high frequency are good only only in the quadrature modulation circuit 134 in a tail end, and, therefore, the adjustment to a frequency is easy for them.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although the adjustable delay means 28 and 41 are used in the former in order to change two path differences, they are this time delay t_A and t_B . It is difficult for a time delay to change according to temperature fluctuation, since the time delay of a line ***** cable is usually used for obtaining, and for delay distortion to arise with a frequency and to change a time delay with large range with still higher resolution.

[0010] Moreover, since it is used, many the balanced modulators 18, 19, 24, 29, 32, 37, 42, 45, 59, and 61, i.e., the multipliers, of high frequency, and the phase shifter of much more RFs is used, the adjustment to a frequency is difficult. And two systems were used and the configuration was complicated.

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MEANS

[Means for Solving the Problem] According to this invention, a transmitting sign is delayed from a sign delay means in step. The first real part, the first imaginary part and the second real part, and the second imaginary part about each sign of the two delay outputs The first, It is changed by the second coordinate operator stage. These first real part and the first imaginary part, respectively with the cosine wave output from the first digital synthesizer, and a sinusoidal output The first, It multiplies with the second multiplication means, and for a start [these], the output of the second multiplication means is changed into an analog signal, respectively while a noise is imposed by the second multiplication mold DA translation means for a start. on the other hand, the cosine wave output and the sinusoidal output from the second digital synthesizer multiply by the second real part and the second imaginary part with the third and fourth multiplication means, respectively -- having -- these third and fourth multiplication output -- the third and fourth multiplication mold DA translation means -- the above -- things -- it is changed into an analog signal while a noise multiplies. For a start, the output of the third DA translation means is added with the first addition means, the output of the second, third, and fourth DA translation means is added with the second addition means, and quadrature modulation of the output of the second addition means is carried out with a quadrature modulation means for a start [these].

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EXAMPLE

[Example] The example of this invention is shown in drawing 1. Transmit information [from the quadrature modulation machine 71] $\theta(t)$ is supplied to the sign delay means 72, and the sign unit, i.e., step-delay, is performed. As for the sign delay means 72, a shift register, a FIFO memory, etc. are used. Moreover, as a quadrature modulation machine 71, dividing of the clock for data generating from the clock generation machine 73 for data generating is carried out to one half with a counting-down circuit 74, counting of the dividing output is carried out with an address counter 75, the memory 76 for inphases and the memory 77 for a rectangular cross are read considering the enumerated data of the address counter 75 as the address, respectively, and in-phase signal $I(t)$ and rectangular signal $Q(t)$ is outputted. both [these] outputs supply a modulator 81 through changeover switches 78 and 79, respectively — having — subcarrier length — for example, a pair-fourth-Differential-QPSK modulation is carried out. Switches 78 and 79 are changed when inputting the in-phase signal and the rectangular signal from the outside. [0013] the sign delay means 72 — respectively — a sign unit — things — delay was given or the signal with which the same delay was given is outputted. The output from a tap (shift stage) which is different when the sign delay means 72 is a shift register, or the output from the same tap (shift stage) is sign transmit information θ_A , respectively. $\langle t \rangle$ and θ_B It is taken out as $\langle t \rangle$ and the coordinate transformation means 82 and 83 are supplied. In the coordinate transformation means 82 and 83, conversion of a polar coordinate and rectangular coordinates is performed and, as for each input sign, real part and imaginary part are outputted, respectively. The real part and imaginary part from the coordinate transformation means 82 are supplied to multipliers 86 and 87 through the FIR form digital low pass filters 84 and 85 if needed, respectively. Moreover, the real part and imaginary part from the coordinate transformation means 83 are supplied to multipliers 91 and 92 through the FIR form digital low pass filters 88 and 89 if needed, respectively.

[0014] On the other hand, the digital synthesizers 93 and 94 are formed. The digital synthesizers 93 and 94 are constituted, as it can change and a phase and a frequency are shown in drawing 2 A, respectively. Namely, frequency f_R from the flip-flop 95 of a toggle mold While was set to one half and the output of an adder 97 is latched to a latch circuit 96 with an output. An adder 97 is the output and the frequency data k_f of a latch circuit 96. It adds. Moreover, the output of a latch circuit 96 is added in phase data k_θ and an adder circuit 98, and in a phase-shifting circuit 99, the phase of 0 times or the phase shift of 90 degrees is given, and the output is read to the sinusoidal memory 101, and is supplied as the address. It is latched to a latch circuit 103 by the signal with which the level of each sample point of a sinusoidal form is memorized by the sinusoidal memory 101, and that digital sinusoidal signal by which reading appearance was carried out was latched to the latch circuit 102 by the latch command to a latch circuit 26, and the phase shifted about 180 degrees to this latch command. The output of a latch circuit 102 turns into a digital sine wave output, the output of a latch circuit 103 is latched to the latch and coincidence to a latch circuit 26 by the latch circuit 104, and a digital cosine wave output is obtained from a latch circuit 104. Frequency data k_f Since accumulation is carried out every clock of frequency $f_R / 2$, it is the frequency data k_f . A frequency becomes high, so that it is large, and it is the frequency data k_f . A frequency becomes low, so that it is small. What is

necessary is just to change whether the most significant bit of the input data and the following bit are passed as it is, or what made what took the exclusive OR for them the most significant bit, and reversed the 2nd bit from the most significant is outputted as 2nd bit from the most significant, as shown in drawing 2 B since a phase-shifting circuit 99 is outputted as it is or a phase is shifted and outputted about 90 degrees. Thus, for a frequency, $f_R \times k / 2L + 1$ and a phase θ are $2\pi k \theta / 2L$. A sinusoidal output and a cosine wave output are obtained. f_R It is the frequency of the clock which drives a flip-flop 95.

[0015] It returns to explanation of drawing 1, frequency $f_1 + f_a$ is set up to a synthesizer 93, phase θ_{1a} is set up, the cosine wave output $\cos \{2\pi(f_1 + f_a) t + \theta_{1a}\}$ is outputted by this, a multiplier 86 is supplied, and the sinusoidal output $\sin \{2\pi(f_1 + f_a) t + \theta_{1a}\}$ is outputted, and a multiplier 87 is supplied. On the other hand to a synthesizer 94, frequency $f_1 + f_b$ is set up, phase θ_{1b} is outputted, the cosine wave output $\cos \{2\pi(f_1 + f_b) t + \theta_{1b}\}$ is supplied to a multiplier 91, and the sinusoidal output $\sin \{2\pi(f_1 + f_b) t + \theta_{1b}\}$ is supplied to a multiplier 92. Each output of multipliers 86 and 87 is supplied to multiplication mold DA converter 105, 106, respectively, and each output of multipliers 91 and 92 is supplied to multiplication mold DA converter 107, 108, respectively. On the other hand, random noise is generated from the random noise generator 109, and after decreasing the noise with an attenuator 111 if needed, while being added in the direct current voltage and the adder circuit 113 from adjustable DC power supply 112, supplying the output of the adder circuit 113 to each criteria power supply terminal of multiplication mold DA converter 105, 106 as Rayleigh noise $A(t)$ and multiplying by it with the input digital signal, the digital signal is changed into an analog signal. The noise from a noise generator 109 is similarly supplied to an adder 115 through an attenuator 114, the output direct current voltage of adjustable DC power supply 116 is added, the output from an adder 115 is supplied to the criteria power supply terminal of multiplier DA converter 107, 108 as Rayleigh noise $B(t)$, and while multiplying to the input digital signal, the digital signal is changed by the analog signal.

[0016] each output of DA converter 105, 106 -- respectively -- an attenuator 117, 118 -- setting -- respectively -- every $[G_a]$ -- it decreases -- having -- moreover, each output from DA converter 107, 108 -- an attenuator 119, 121 -- setting -- respectively -- G_B only -- it decreases. The output of an attenuator 117, 119 is added in an adder 122, and is supplied to a multiplier 123, and each output of an attenuator 118, 121 is added with an adder 124, and is supplied to a multiplier 125.

[0017] the signal from the reference signal generator 126 -- frequency f_R it is -- while synthesizers 93 and 94 are supplied as a clock, respectively, dividing of the output is carried out to 1 for an integer by the counting-down circuit 127, while the clock generation machine 27 for data generating is supplied, it is supplied as a shift clock to the sign delay means 72, and each part is supplied as a clock for other digital processings. Furthermore, the output of the reference signal generator 126 is supplied to a phase locked loop (PLL) 128 as a reference signal. In the PLL 128, it is carrier frequency $f_0 - f_1$. A setting-out input is carried out. Frequency $f_0 - f_1$ which synchronized with the reference signal $\text{Signal} \cos \{2\pi(f_0 - f_1) - t\}$ is outputted, and while this is supplied to a multiplier 123 as a carrier signal, a multiplier 125 is supplied through a phase shifter 129 90 degrees. The output of a multiplier 123, 125 is added with an adder 131, and the addition output is decreased with an attenuator 132, and is outputted to an output terminal 133. The multiplier 123, 125, the phase shifter 129, and the adder 131 constitute the quadrature modulation circuit 134. Moreover, it is the output carrier frequency of PLL 128 $f_0 - f_1$ What is carried out is the carrier frequency f_0 of the output signal of an output terminal 133. It is necessary to increase or to decrease. that is, -- since a negative frequency cannot be generated in synthesizers 93 and 94 -- f_1 only -- as a high frequency It is a core f_0 about the frequency of an output subcarrier [in / by this / forward and the negative frequencies f_a and f_b can be freely chosen to it, and / the quadrature modulation circuit 13]. It can receive and only f_a and f_b can change to forward and negative.

[0018] In this configuration, a shift register is used for the sign delay means 72, and it is f_d about that shift frequency. If it carries out and the shift stage where an output is taken out is set to n_a and n_b , the sign information supplied to the coordinate transformation means 82 and 83 is

thetaA, respectively. $\theta(t) = \theta(t - n_a/f_d)$ and θ_B It is set to $\theta(t) = \theta(t - n_b/f_d)$. Therefore, the signal outputted with a terminal 133 is as follows.

[0019] $G_c = [2\pi(f_0 + f_a)$ and $G_a = A(t)$ and $\cos\{t + \theta_a + \theta(t - n_a/f_d)\} + G_b = B(t)$, and $\cos\{2\pi(f_0 + f_b)$ and $t + \theta_b + \theta(t - n_b/f_d)\}]$

In the case of a phasing simulation, it is two modulation-codes [the same shift stage in the sign election means 72 to] $\theta_A(t)$ and $\theta_B(t)$ is obtained or it is modulation-code $\theta_A(t)$ and $\theta_B(t)$ shifts the amount of delay only in the condition of maintaining correlation.

Rayleigh scattering over the path of two electric waves is given as $A(t)$ and $B(t)$, and a value with each Doppler shift respectively small as f_a and f_b in the first electric-wave path and second electric-wave path is given. The phase contrast of the two electric-wave paths is determined by setting-out phase θ_{aa} in the digital synthesizers 93 and 94, and θ_{ab} , the Rayleigh noise is given by $A(t)$ and $B(t)$, and the magnitude of attenuation is changed by the attenuator 117,119. The time delay of the first electric-wave path is given by $\{(n_a/f_d) - \theta_{aa} / 2\pi(f_0 + f_a)\}$, and the time lag of the second electric-wave path is given by $\{(n_b/f_d) - \theta_{ab} / 2\pi(f_0 + f_b)\}$. The signal with which each part was controlled and the phasing effectiveness was given like the conventional technique can be acquired by doing in this way.

[0020] Moreover, two signals θ_A which sets for the sign delay means 27 and is outputted more when acquiring the interference signal between adjacent channels $\theta(t)$ and θ_B In order that $\theta(t)$ may make the difference of the amount of delay size mutually at extent without correlation and may obtain the delta frequency between channels in the condition, a part of setting-out frequency f_a and f_b of synthesizers 93 and 94 is detached enough mutually. Also in this case, the simulation of the interference signal between adjacent channels can be carried out as usual.

[0021] In ***, the simulation of multi-pass phasing and the interference simulation between other a large number channels can be performed by preparing two or more groups of the coordinate transformation means 82, filters 84 and 85, multipliers 86 and 87, DA converter 105,106, an attenuator 111, an adder 113, an attenuator 117,118, and a power source 112. Moreover, in ***, although the phasing simulation about a pair-fourth-Differential-QPSK modulating signal was performed, the simulation of phasing to other communication modes or interference between adjacent channels can also be performed by changing a modulator 71.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The block diagram showing the example of this invention.

[Drawing 2] The block diagram in which A shows the example of a digital synthesizer, and B are the block diagrams showing the phase-shifting circuit 99.

[Drawing 3] The block diagram showing the conventional phasing simulator.

[Translation done.]